



NARULA INSTITUTE OF TECHNOLOGY

81, Nilgunj Road, Agarpara, Kolkata- 700109

REPORT ON
SEMESTER/ CONFERENCE / WORKSHOP

1. Name of the Participant : SURAJIT BARI
(in block letter)
2. Department : ECE 3. Designation: Assistant Professor
4. Category : Faculty TA Other Staff
5. Sponsorship : NIT Self
6. Title of the Seminar : International Summer and Winter Term (ISWT) course on “Advanced Formal Techniques in Design, Verification and Testing of Digital Integrated Circuits”
7. Seminar Organized by IIT, Kharagpur
8. Duration : 16th -27th June,2014 9. Total Participant: 38
10. Topic Discussed
 1. Introduction to formal techniques in design and verification,
 2. Advances in formal verification techniques,
 3. Formal techniques in debugging and testing
 4. Reversible circuit synthesis using formal techniques
11. Name of the speakers (with Contact Nos. , if possible)
 1. Prof. Indranil Sen Gupta (Course Coordinator),Department of Computer Sc. & Engg. IIT, Kharagpur
 2. Prof.Pilab Dasgupta(Course Co- Coordinator) Department of Computer Sc. & Engg. IIT, Kharagpur
 3. Prof. Rolf Drechsler , University of Bremen ,Germany
 4. Prof. Supratik Chakraborty, Department of Computer Sc. & Engg. IIT, Bombay

12. Name of the Other Participating Institutes:

1. IIT, Kharagpur
2. ISI, Kolkata
3. NIT, Meghalaya
4. IEM, Kolkata
5. NSEC, Kolkata
6. M/S Intel
7. M/S Synopsys

13. Brief report on the deliberation of the Seminar (to be attached as Annexure-1) :

14. Presentation given at NIT on 7th July, 2014

15. Presentation Attended by : Faculty Students

Date:

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Signature of the Participant

Comments by HOD (with special emphasis on how NIT has been benefited):

After attaining the International Summer & Winter Term Course on “Advanced Formal Techniques in Design, Verification and Testing of Digital Integrated Circuits” at IIT, Kharagpur, India, Mr. Surajit Bari has presented and discussed about the overview of recent advancement of formal verification techniques and testing of digital VLSI circuits near to the faculty members and students. Physical Design & Testing is one of the papers included in M-Tech (VLSI) syllabus so PG students have been indirectly benefitted and will also be benefitted in future context to their course curriculum and also in project. UG students have also been benefitted as VLSI paper is included in their course curriculum. Interested faculty members in the specific field have also got idea about the recent development of VLSI and techniques of formal verification in VLSI circuits.

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Signature of HOD

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Signature of Principal

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Signature of Director

Report on

International Summer and Winter Term (ISWT) course on “Advanced Formal Techniques in Design, Verification and Testing of Digital Integrated Circuits”

From 16th -27th June, 2014

Organized by IIT, Kharagpur at IIT, Kharagpur

Name of the Participant: Surajit Bari, Assistant Professor,
ECE Department, Narula Institute of Technology, Agarpara, Kolkata

Introduction: The objective of the course is to focus on advancement of formal techniques in design verification and testing of digital integrated circuits. Prof. Indranil Sen Gupta (Course Coordinator), Department of Computer Sc. & Engg. IIT, Kharagpur; Prof. Pllab Dasgupta (Course Co-Coordinator) Department of Computer Sc. & Engg. IIT, Kharagpur; Prof. Rolf Drechsler, University of Bremen, Germany; Prof. Supratik Chakraborty, Department of Computer Sc. & Engg. IIT, Bombay have delivered their lecture in different domain of formal verification and testing of digital VLSI circuits. Topics like design flow of IC, Succinct Representations of Finite-State Systems, Languages, Model checking techniques, power intent, Hardware software co verification, reversible circuits, test generation, fault diagnosis have been discussed during the course. Laboratory sessions have also been conducted to meet the research, development & experimental aspects of formal verification and fault modeling. Two examinations have also been conducted in the course schedule. Faculty members, Industry experts, Researchers and Students from different institutes/organizations have participated in the course. During each session of both Lecture and Laboratory recent direction of research on formal verification and testing of digital VLSI circuits have been explored.

Description: Entire course content is divided into four parts. Part I: Introduction to formal techniques in design and verification, Part II: Advances in formal verification techniques, Part III: Formal techniques in debugging and testing, Part IV: Reversible circuit synthesis using formal techniques.

Prof. Sengupta in his introductory lecture on 1st day of course has focused on IC design flow like specification -> synthesis -> simulation -> layout -> testability analysis. He also added about behavioral design, data path design, logic design, physical design, manufacturing. Design level at behavioral, structural and physical level has been mapped using Y-Chart. Idea of logic synthesis and Technology mapping has also been discussed. Inputs of logic synthesis are Boolean equations and FSMs. Output of logic synthesis is net list of gates and flip flop. Logic synthesis is done to meet the design goals by minimizing the numbers of levels (delay), numbers of gate (area) and signal activity (power).

Prof. Chakraborty has delivered lecture basically on two topic (i) Succinct Representation and (ii) Model checking. He has pointed out on FSM, Characteristics functions. There are two category of

succinct representation: (a) BDD(Binary Decision Diagram) -> ROBDD(Reduced Order Binary Decision Diagram) which is canonical representation and used for constant time satisfiability /tautology checking ,also works for a large class of industrial problems.(b) Functionally Reduced And-Inverter Graphs (FRAIGs) : This is non-canonical representation , used for NP-complete satisfiability checking and geared towards SAT based techniques. For ROBDD if-then-else (ite) operator and variable ordering problem have been explained. Equivalence checking using BDD is discussed.

Following topics have been discussed by Prof. Chakraborty under Model Checking Techniques.

- What is model checking
- Modeling basics
- Property specification in temporal logic
- CTL model checking
- LTL model checking

Prof. P. Dasgupta has delivered lectures on (i) languages and formalism (ii) Abstractions, refinements and coverage in formal verification (iii) Formal verification of power intent and (iv) Hardware/software co-verification.

In his 1st lecture, Prof. Dasgupta has focused on Omega regular language, automata over infinite words, temporal operators. There are four temporal operators: the next operator, the until operator, the eventual operator, the always operator. In the 2nd lecture Prof. Dasgupta Delivered on cone of influence, abstract input space, property level abstractions and on formal verification coverage .In the next lecture prof. Dasgupta pointed out on different power spent in CMOS and low power design issues through formal verification technique. In the last lecture formal methods for hardware software Co-verification have been added by Prof.Dasgupta.In this lecture he basically discussed on firmware , bounded model checking ,HW-CBMC ,K-induction etc.

Prof. Rolf Drechsler has delivered lectures on reversible circuit synthesis using formal techniques .Following topics have been discussed by Prof. Drechsler.

- Reversible logic
- Truth table based synthesis
- Exact synthesis
- ESOP- based synthesis
- BDD- based synthesis

He nicely presented the concept of CNOT gate, Toffoli gate and Fredkin gate to realize reversible circuit and about synthesis of circuit.

Prof. I. Sen Gupta also delivered lectures on simulation and formal verification, testing, formal techniques in test generation and, formal techniques in fault diagnosis. He explain about three valued truth table ,logic /True-value Simulation , Compiled code simulation and Event driven simulation using nice example.

In his lectures following major topics have been discussed.

- Verification vs. Testing
- Necessity and level of testing
- Fault coverage
- Basic testing principle
- Stuck –at fault model
- Delay fault
- Generation of CNF for SAT solver
- Simulation Based fault diagnosis
- SAT based diagnosis

In the laboratory sessions formal methods for verification and testing have been demonstrated. BDD approach, satisfiability checking, hardware-software co-verification, fault modeling etc. have been practiced.

Conclusion: From the two week course from 16th to 27th June,2014 recent approach of formal verification techniques for digital VLSI circuits have been explored. Topics like: Introduction to formal techniques in design and verification , Advances in formal verification techniques , Formal techniques in debugging and testing , Reversible circuit synthesis using formal techniques have been delivered by the speakers with their best effort . New ideas of teaching, learning and research have been obtained through the course.

References: Class notes and study material provided by the IIT, Kharagpur.

Acknowledgement: I am very much thankful to IIT, Kharagpur to organize such course and giving me the opportunity to participate in the course. My respect to all the Speakers of the course. My thanks to all the members of IIT, Kharagpur associated with the course. I am very much grateful to Narula Institute of Technology, JIS Group, Kolkata and ECE Department ,NIT for giving me the permission to attain the course through Technical Education Quality Improvement Program (TEQIP),Pase-II, Sub Component 1.1.

Signature: Surajit Bari

Date:

Place:

